**Amendments to the Specification**

Please delete the paragraph starting at page 4, line 31 that begins with the words "Based on this prior art . . .".

Please amend the paragraph that begins at page 4, line 35 with the following:

An embodiment of the ~~The~~ present invention is a semiconductor device having a substrate, an active area formed within the substrate, a first non-planar metallization level which is formed on the substrate and is in contact with the active area and a second planar metallization level arranged spaced apart from the first metallization level above the substrate and connected to the first metallization level via a through connection.

Please amend the paragraph that begins at page 7, line 35 with the following:

~~According to the invention, thus, as it may be seen from~~ As shown, for example, in Fig. 2, the ~~proceedings~~ advantageous structures described above with reference to Fig. 1A and 1b are combined in the illustrated transistor. The first metallization level is not planar, whereby good shielding of the gate is achieved. In the drain area, this metallization level is ended due to the field oxide 26 before possibly ~~setting~~ forming steps~~,~~. The ~~the~~ conductive trace ~~according to~~ portion 42b is thus not implemented so far that it extends in steps over the field oxide 26 in the right area of Fig. 2. Via vias (plugs between metal levels) the second metallization level is connected to the conductive trace

portion 42b of the first metallization level. ~~It~~ The second metallization level carries the current out of the ~~finger~~ the conductive trace portion 42b of the first metallization level and is planar.

Please amend the paragraph that begins at page 8, line 17 with the following:

Figs. 3 and 4 are schematical illustrations of a vertical section through a field effect transistor according to a preferred embodiment of the present invention. ~~At that time~~, Fig. 4 is an ~~expanded~~ enlarged illustration of a section of Fig. 3.

Please amend the paragraph that begins at page 12, line 27 with the following:

In the preferred embodiment illustrated in Figs. ~~1 and 2~~ 2-4, the LOCOS layer 26 preferably comprises a thickness of 33 nm. The oxide layer 26 is preferably an HDP oxide (HDP = high density plasma) with a thickness of 2.5 μm to 3 μm. The laterally sturctured metal layer preferably comprises titanium Ti or titanium nitride TiN or aluminum. While Titanium and titanium nitride ~~comprise~~ exhibit a higher specific resistance, they may, however, be applied without a barrier onto a silicon surface. Aluiminum ~~comprises~~ exhibits a lower specific resistance, but a barrier layer is ~~to be provided, however,~~ typically required between aluminum and a silicon surface.